深圳市高信技术有限公司
Shenzhen G&X Technology Co., Ltd

# SPECIFICATION
# FOR
# LCD MODULE

Customer :

CustomerP/N

Model No. : GX05S-30MI-A1

Version : V01

Date : 2026-03-02

**Final Approval by Customer**

| Approved by | Notes |
|---|---|
| | |

**ShenZhen GX Confirmed :**

| Prepared by | Checked by | Approved by |
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## 1.Record of Revision

| Rev. | Issued Date | Description | Editor |
|---|---|---|---|
| 1.0 | 2026-03-04 | First release | CHEN |
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## 2.General Specifications

Note 1: Viewing direction for best image quality is different from TFT definition. There is a 180°shift.

Note 2: RoHs compliant.

| Item | Specification | Unit |
|---|---|---|
| LCD size | 5.08 | inch |
| Display Mode | Normally Black | -- |
| Resolution | 720(RGB)x720 | Pixel |
| Pixel pitch | 0.1269*RGB*0.1269 | mm |
| Pixel Arrangement | RGB Stripe | |
| Viewing direction | ALL | - |
| Module outline dimension | 93.67(H)*96.87(V)*2.15(D) | mm |
| LCD AA | 91.368*91.368 | mm |
| Colors | 16.7M | - |
| Driver IC | JD9365TX | - |
| Interface | MIPI 4lane | -- |
| Backlight | White LED | -- |
| Operating Temperature | -20℃~ +70℃ | -- |
| Storage Temperature | -30℃~ +80℃ | -- |

## 3.Pin Assignment

| PIN | Symbol | Description | Remark |
|---|---|---|---|
| 1 | LEDA | LED ANODE | |
| 2 | LEDK1 | LED CATHODE | |
| 3 | LEDK2 | LED CATHODE | |
| 4 | VCI | power supply 3.3V | |
| 5 | IOVCC | power supply | |
| 6 | RESET | Reset pin. Setting either pin low initializes the LSI. Must be reset (active low) after power is supplied | |
| 7 | TE | Serves TE (Tearing Effect) pin of each scan line | |
| 8 | PWM | Backlight on/off control pin | |
| 9 | GND | Ground | |
| 10 | D0P | MIPI-DSI Data differential signal input pins | |
| 11 | D0N | MIPI-DSI Data differential signal input pins | |
| 12 | GND | Ground | |
| 13 | D1P | MIPI-DSI Data differential signal input pins | |
| 14 | D1N | MIPI-DSI Data differential signal input pins | |
| 15 | GND | Ground | |
| 16 | TCP | MIPI-DSI CLOCK differential signal input pins | |
| 17 | TCN | MIPI-DSI CLOCK differential signal input pins | |
| 18 | GND | Ground | |
| 19 | D2P | MIPI-DSI Data differential signal input pins | |
| 20 | D2N | MIPI-DSI Data differential signal input pins | |
| 21 | GND | Ground | |
| 22 | D3P | MIPI-DSI Data differential signal input pins | |
| 23 | D3N | MIPI-DSI Data differential signal input pins | |
| 24 | GND | Ground | |
| 25 | TP-INT | Touch Interrupt | |
| 26 | TP-SDA | Touch IIC Data signal | |
| 27 | TP-SCL | Touch IIC Clock signal | |
| 28 | TP-RESET | Touch Reset Signal | |
| 29 | NC | NC | |
| 30 | GND | Ground | |

## 4.Absolute Maximum Ratings

| Item | Symbol | Min. | Max. | Unit | Remark |
|---|---|---|---|---|---|
| Power Voltage | VCI | / | +3.3 | V | |
| | IOVCC | +1.65 | +1.95 | V | |
| | TP_VCI | / | / | V | |
| | TP_IOVCC | / | / | V | |
| Operating Temperature | Top | -20.0 | 70.0 | ℃ | |
| Storage Temperature | $T_{st}$ | -30.0 | 80.0 | ℃ | |
| Operating and Storage Humidity | $H_{stg}$ | 10% | 90% | %(RH) | |

## 5.Electrical Characteristics

### 5.1Recommended Operating Condition

| Item | | Symbol | Min. | TYP. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|---|
| Digital supply Voltage | | IOVCC | 1.65 | / | 1.95 | V | |
| Analog supply Voltage | | VCI | / | 3.3 | / | V | |
| TP Power | | TP_VCI | / | / | / | V | |
| TP Power | | TP_IOVCC | / | / | / | V | NOTES |
| Input Signal Voltage | Low Level | $V_{IL}$ | 0 | - | 0.3 x IOVCC | V | |
| | High Level | $V_{IH}$ | 0.7 x IOVCC | - | IOVCC | V | |
| Current of digital supply voltage | | $I_{IOVCC}$ | - | / | / | Ma | |
| Current of analog supply voltage | | $I_{VCI}$ | - | / | / | Ma | |

## 5.2 Backlight Unit Driving Condition

| Item | Symbol | Min. | TYP. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|
| Forward Current | $I_F$ | - | 80 | - | Ma | |
| Forward Current Voltage | $V_F$ | - | 15 | - | V | |
| Operating Life Time | -- | 20000 | -- | -- | hrs | Note 2, Note 3 |

Note1: The LED driving condition is defined for each module.

Note2: When LCM is operated, the stable forward current should be inputted. And forward voltage is for reference only.

Note3: Optical performance should be evaluated at Ta=25℃ When LED is driven at high current, high ambient temperature & humidity condition. The life time of LED will be reduced. Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.

Note4: The LED driving condition is defined for each LED module.

# 6.Timing Characteristics

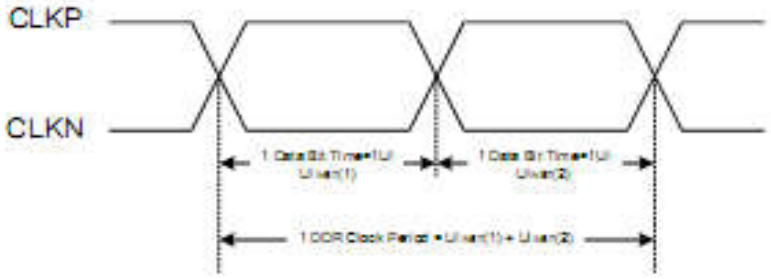
## 6.1 Interface Characteristics :

**High-Speed Data-Clock Timing**

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction. In either the Forward or Reverse signaling modes there shall be only one clock source. In the Reverse direction, Clock is sent in the Forward direction and one of four possible edges is used to launch the data.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term "rising edge" means "rising edge of the differential signal, i.e. CLKP – CLKN, and similarly for "falling edge". Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown in Figure 13.5.




**DDR Clock Definition**

The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

The UIINST specifications for the Clock signal are summarized in following Table.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| UI instantaneous | $UI_{INST}$ | - | - | 12.5 | ns | (1), (2), (3), (4), (5), (6) |

**Note:** (1) This value corresponds to a minimum 80 Mbps data rate.
(2) The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.
(3) Maximum total bit rate is 1.7Gbps of 2 data lanes 24-bit data format/ 1.27Gbps of 2 data lane 18-bit data format/ 1.13Gbps of 2 data lane 16-bit data format.
(4) Maximum total bit rate is 2Gbps of 3 data lanes 24-bit data format/ 1.5Gbps of 3 data lane 18-bit data format/ 1.33Gbps of 3 data lane 16-bit data format.
(5) Maximum total bit rate is 2Gbps of 4 data lanes 24-bit data format/ 1.5Gbps of 4 data lane 18-bit data format/ 1.33Gbps of 4 data lane 16-bit data format.

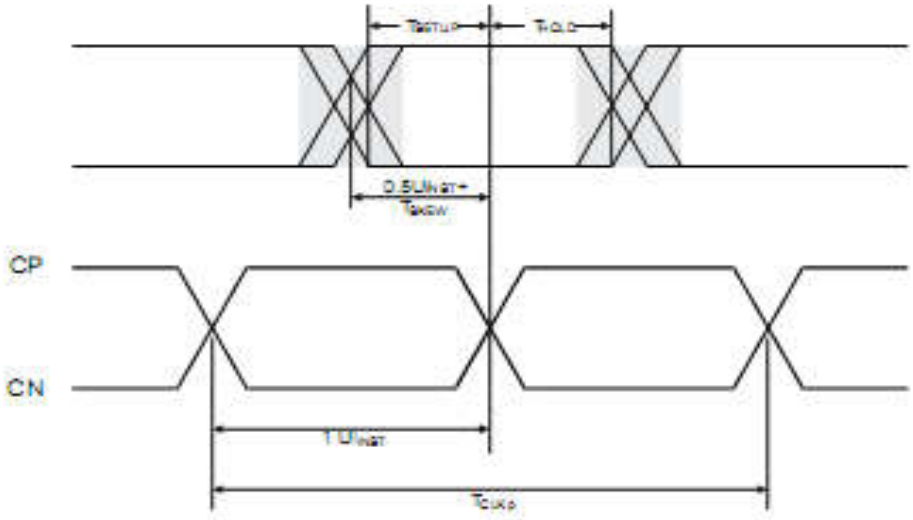
**Table 11.11: Reverse HS Data Transmission Timing Parameters**

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 8.13. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.

The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.

All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.




**Data to Clock Timing Definitions**

## Data-Clock Timing Specifications

The Data-Clock timing specifications are shown in Table 13.12. Implementers shall specify a value $UI_{INST,MIN}$ that represents the minimum instantaneous UI possible within a High-Speed data transfer for a given implementation. Parameters in Table 13.12 are specified as a part of this value.. The setup and hold times, $T_{SETUP[RX]}$ and $T_{HOLD[RX]}$, respectively, describe the timing relationships between the data and clock signals. $T_{SETUP[RX]}$ is the minimum time that data shall be present before a rising or falling clock edge and $T_{HOLD[RX]}$ is the minimum time that data shall remain in its current state after a rising or falling clock edge. The timing budget specifications for a receiver shall represent the minimum variations observable at the receiver for which the receiver will operate at the maximum specified acceptable bit error rate.

The intent in the timing budget is to leave $0.4*UI_{INST}$, i.e. $\pm 0.2*UI_{INST}$ for degradation contributed by the interconnect.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| Data to Clock Setup Time [RX] | $T_{SETUP[RX]}$ | 0.15 | - | - | $UI_{INST}$ | (1) |
| Clock to Data Hold Time [RX] | $T_{HOLD[RX]}$ | 0.15 | - | - | $UI_{INST}$ | (1) |

**Note:** (1) Total setup and hold window for receiver of $0.3*UI_{INST}$.

**Data to Clock Timing Specifications**

## Burst Mode Data Transmission

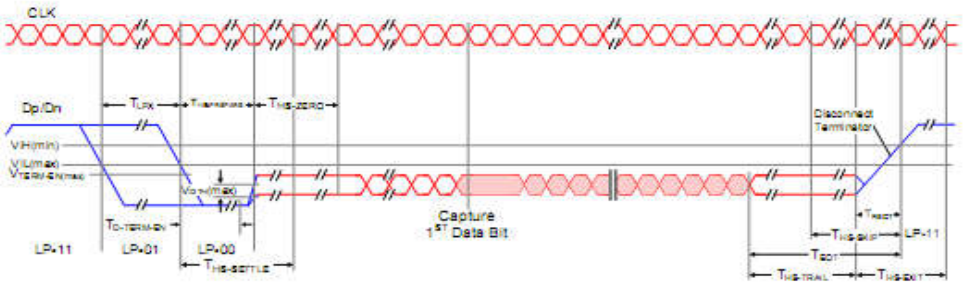



**Figure 11.8: High-Speed Data Transmission in Bursts**

| Parameter | Description | Min | Typ | Max | UNIT |
|---|---|---|---|---|---|
| $T_{LPX}$ | Transmitted length of any Low-Power state period | 50 | - | - | ns |
| $T_{HS-PREPARE}$ | Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission | 40 + 4*UI | - | 85 + 6*UI | ns |
| $T_{HS-PREPARE}$ + $T_{HS-ZERO}$ | $T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence. | 145 + 10*UI | - | - | ns |
| $T_{D-TERM-EN}$ | Time for the Data Lane receiver to enable the HS line termination. | - | - | 35 + 4*UI | ns |
| $T_{HS-SETTLE}$ | Time interval during which the HS receiver shall ignore any Data Lane HS transitions. | 85 + 6*UI | - | 145 + 10*UI | ns |
| $T_{HS-TRAIL}$ | Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst | max( n*8*UI, 60 + n*4*UI ) | - | - | ns |
| $T_{HS-EXIT}$ | Time that the transmitter drives LP-11 following a HS burst. | 100 | - | - | ns |

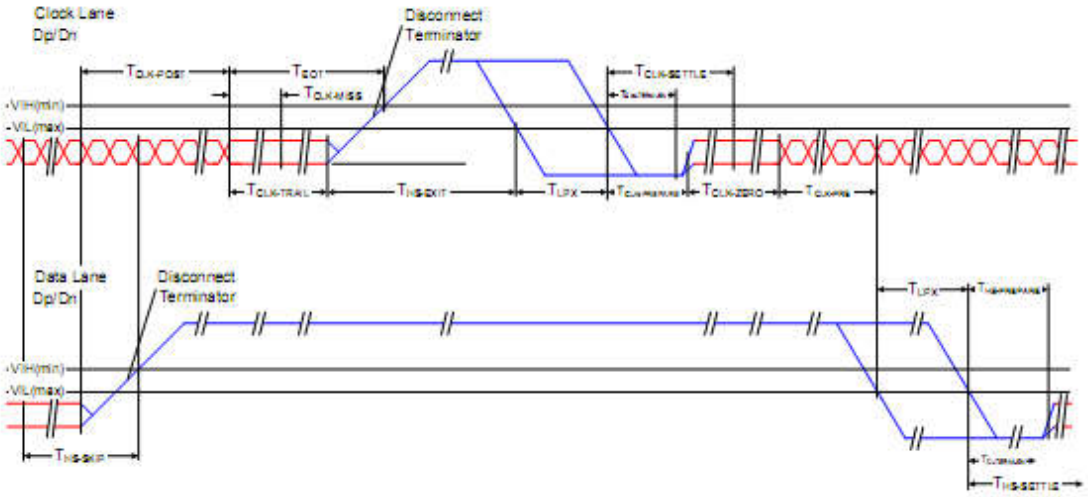
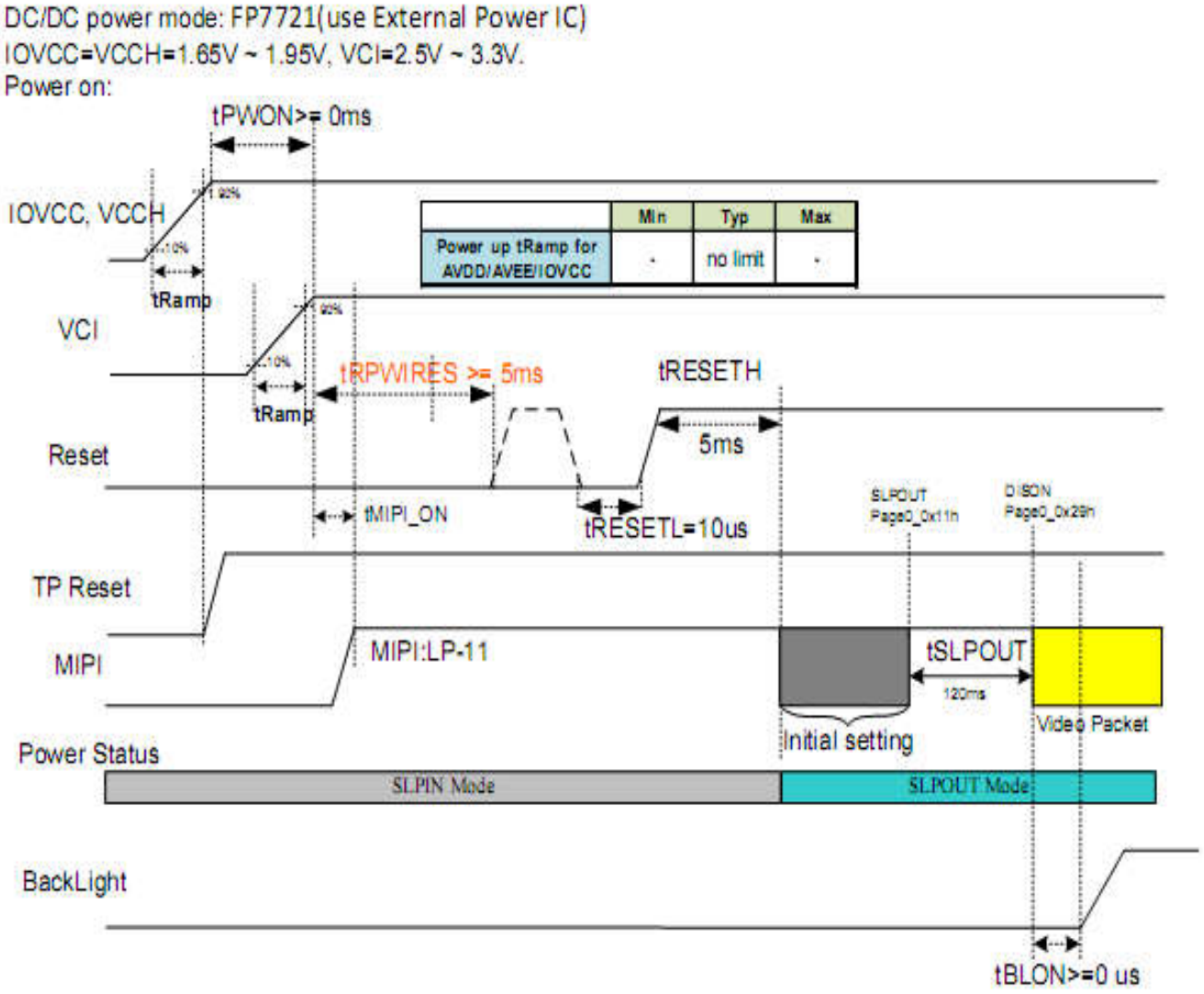



**Figure 11.9: Switching the Clock Lane between Clock Transmission and Low-Power Mode**

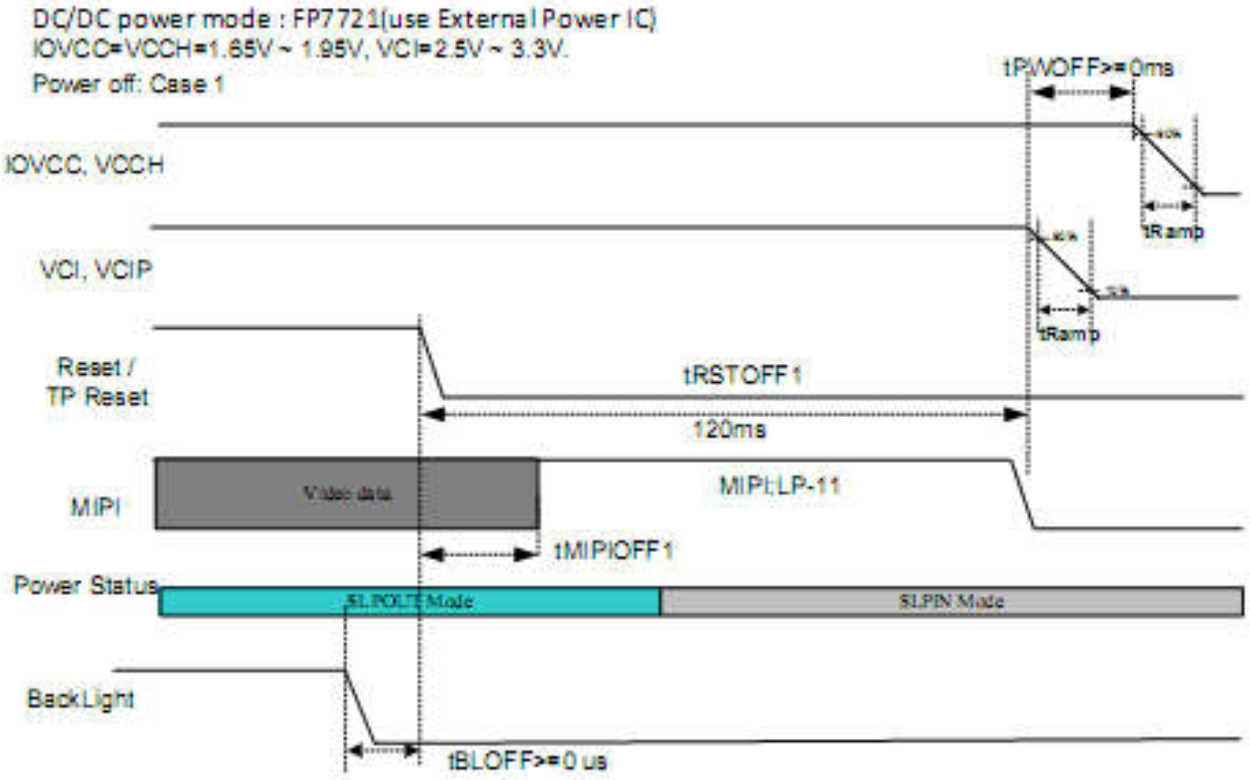
| Parameter | Description | Min | Typ | Max | UNIT |
|---|---|---|---|---|---|
| $T_{CLK-POST}$ | Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. | 60 + 52*UI | - | - | ns |
| $T_{CLK-PRE}$ | Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode. | 8*UI | - | - | ns |
| $T_{CLK-PREPARE}$ | Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission. | 38 | - | 95 | ns |
| $T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$ | $T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock. | 300 | - | - | ns |
| $T_{CLK-TERM-EN}$ | Time for the Clock Lane receiver to enable the HS line termination. | - | - | 38 | ns |
| $T_{CLK-TRAIL}$ | Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst. | 60 | - | - | ns |
| $T_{HS-EXIT}$ | Time that the transmitter drives LP-11 following a HS burst. | 100 | - | - | ns |

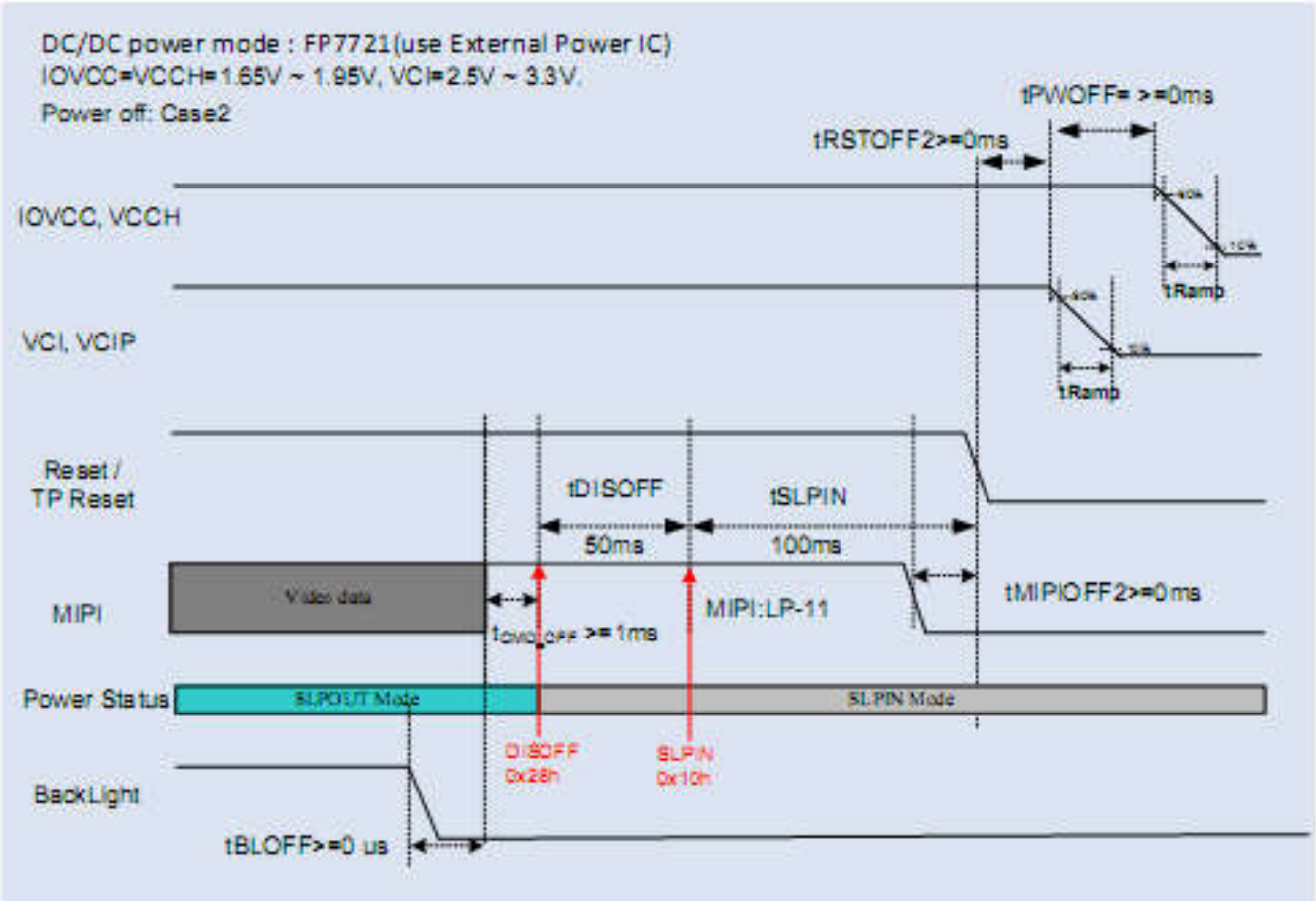
## 6.2 Power On /OFF Timing

Power on sequence



Power off sequence



## 6.3 RESET Timing

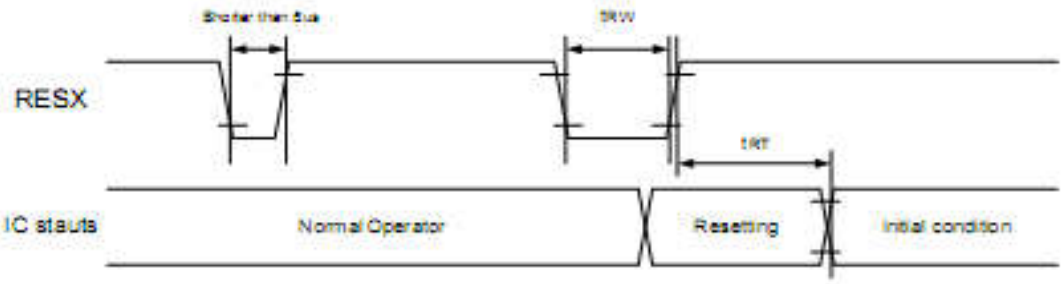



**Figure 11.1: Reset input timings**

| Symbol | Parameter | Related pins | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{RW}$ | Reset pulse width(2) | RESX | 10 | - | µs |
| $t_{RT}$ | Reset complete time(3) | - | - | 5 (Note 5) | ms |
| | | - | - | 120 (Note 6, 7) | ms |

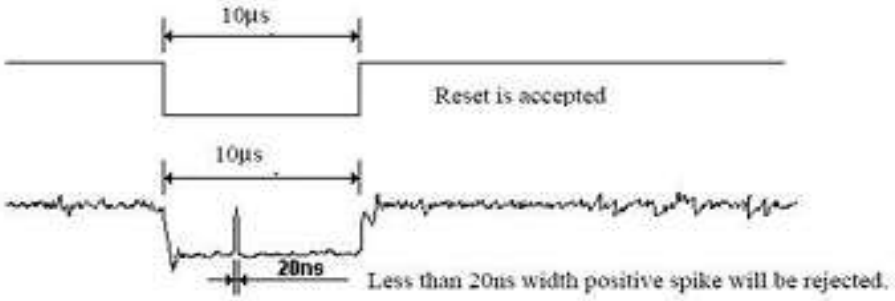
**Note:** (1) The reset complete time also required time for loading ID bytes from OTP to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

(2) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

| RESX Pulse | Action |
|---|---|
| Shorter than 5 µs | Reset Rejected |
| Longer than 10 µs | Reset |
| Between 5 µs and 10 µs | Reset Start |

(3) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for HW reset.

(4) Spike Rejection also applies during a valid reset pulse as shown below:



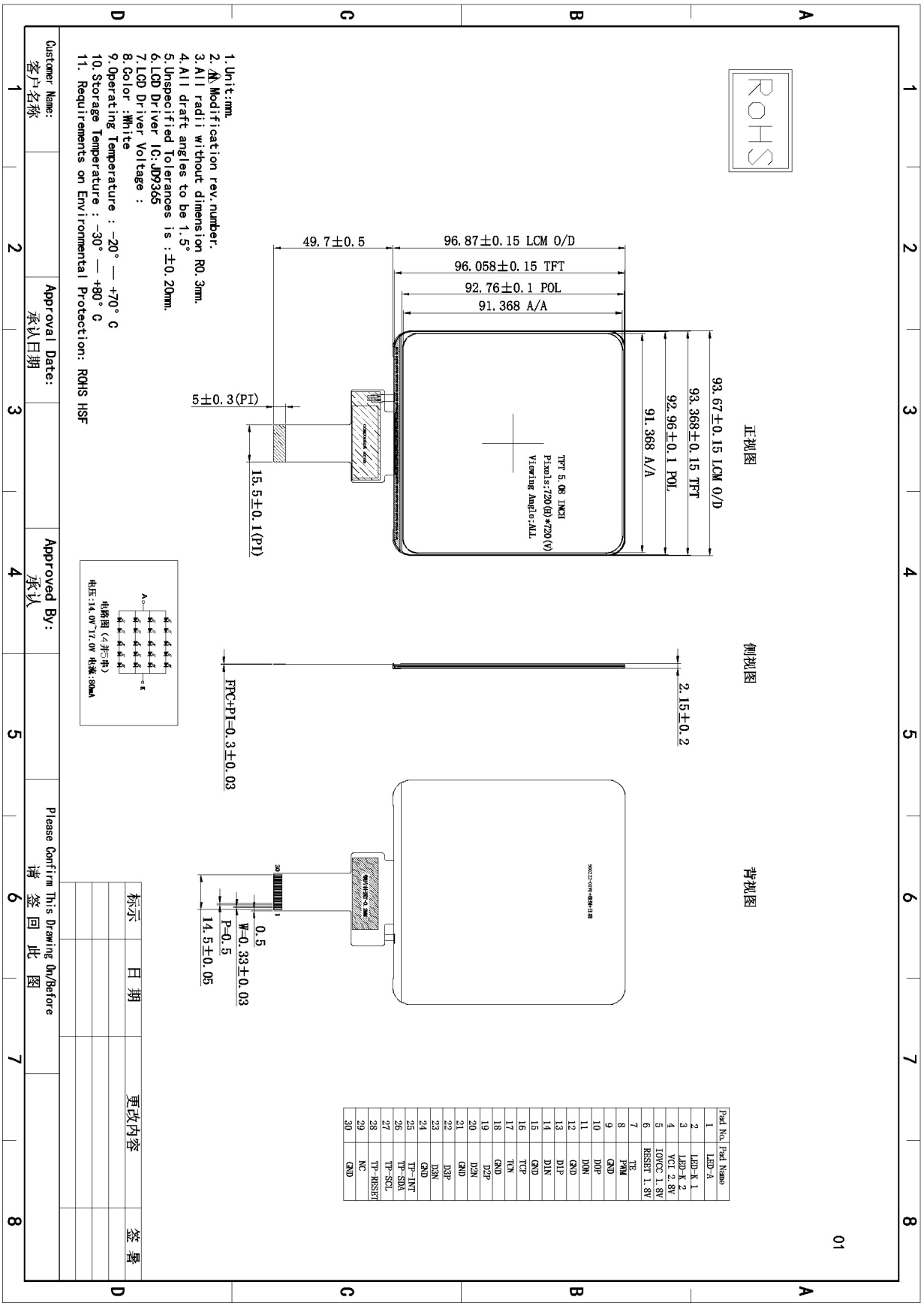

(5) When Reset is applied during Sleep In Mode.

(6) When Reset is applied during Sleep Out Mode.

(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

(8) After Sleep Out Command, it is necessary to wait 120msec then send RESX.

# 7.Mechanical Drawing



## 8.Optical Characteristics

| Item | | Symbol | Condition | Min. | TYP. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|---|---|
| View Angles | | θT | CR≧10 | - | 85 | - | Degree | Note 2 |
| | | θB | | - | 85 | - | | |
| | | θL | | - | 85 | - | | |
| | | θR | | - | 85 | - | | |
| Contrast Ratio | | CR | θ=0° | - | 1200 | - | | Note1 Note3 |
| Response Time | | $T_{ON}$ | 25℃ | | - | 35 | ms | Note1 Note4 |
| | | $T_{OFF}$ | | | | | | |
| Chromaticity | White | x | Backlight is on | - | - | - | | Note1 Note5 |
| | | y | | - | - | - | | |
| Uniformity | | U | | - | 80 | - | % | Note1 Note6 |
| NTSC | | | | - | 65 | - | % | Note 5 |
| Luminance | | L | | - | 460 | - | $CD/m^2$ | Note1 Note7 |

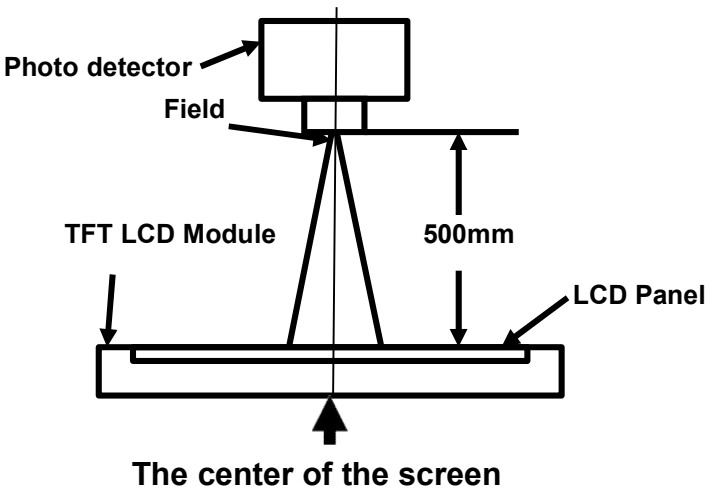
Test Conditions:

1.IF= 80 Ma, VF=15 V and the ambient temperature is 25±2℃.humidity is 65±7%

2.The test systems refer to Note 1 and Note 2.

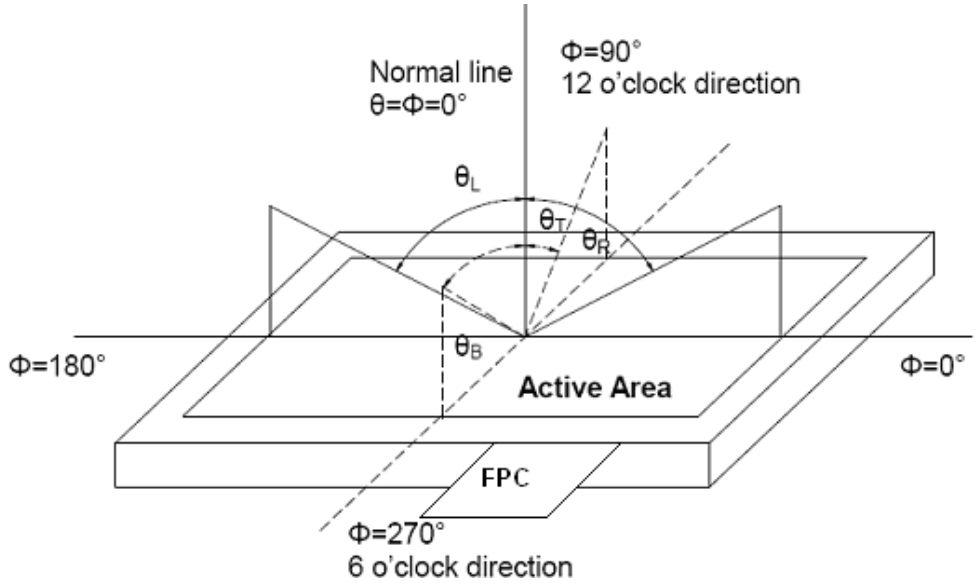
## Note 1: Definition of optical measurement system.

Properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.




## Note 2: Definition of viewing angle range and measurement system.

Viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80)。

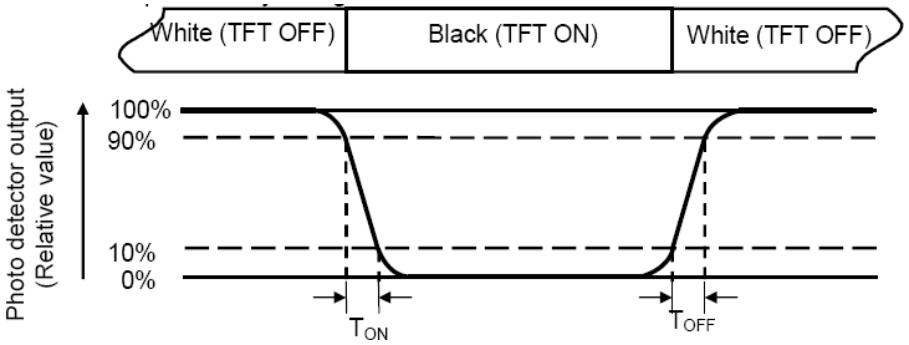



## Note 3: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

## Note 4: Definition of response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time ($T_{ON}$) is the time between photo detector output intensity changed from 90%




to 10%. And fall time ($T_{OFF}$) is the time between photo detector output intensity changed from 10% to 90%.

## Note 5: Definition of color chromaticity (CIE1931)

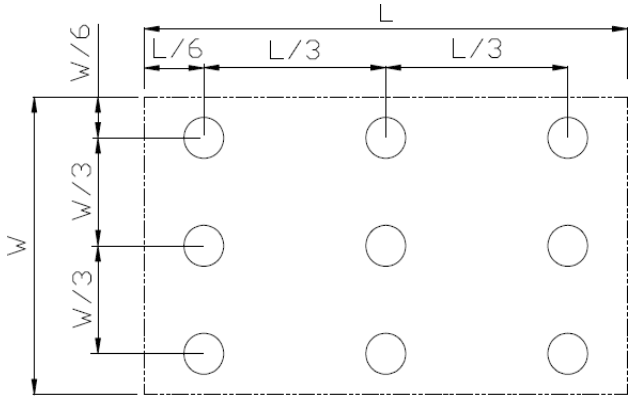
Color coordinates measured at center point of LCD.

## Note 6: Definition of luminance uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = Luminance min / Luminance max

L-------Active area length W----- Active area width




Luminance max: The measured Maximum luminance of all measurement position. Luminance min: The measured Minimum luminance of all measurement position.

## Note 7: Definition of luminance:

Measure the luminance of white state at center point

## 9.Environmental / Reliability Test

| No. | Items | Condition | Inspection after test |
|---|---|---|---|
| 1 | High Temperature Storage | T = 80℃ for 96 hr | Inspection after 4 hours storage at room temperature, the sample shall be free from defects:<br>1.Air bubble in the LCD<br>2.Seal leak;<br>3.Non-display; 4.missing segments; 5.Glass crack;<br>6.Current IDD is twice higher than initial value. |
| 2 | Low Temperature Storage | T = -30 for 96 hr | |
| 3 | High Temperature Operating | T = 70℃for 96 hr | |
| 4 | Low Temperature Operating | T = -20℃ for 96 hr<br>(But no condensation of dew) | |
| 5 | High Temp. and High Humidity Operating | T = 60℃/90% for 96 hr (But no condensation dew) | |
| 6 | Thermal Shock | -20±2℃~25~70±2℃×10cycles<br>(30min.) (5min.) (30min.) | |
| 7 | ESD | Voltage:±2KV R: 330Ω C: 150pF Air discharge, 10time | |

Note1: Ts is the temperature of panel's surface.

Note2: Ta is the ambient temperature of samples

## 10.Precautions for Use of LCD Modules Handling Precautions

### 10.1Handling Precautions

10.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

10.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

10.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

10.1.4 The Polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this Polarizer carefully.

10.1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the Polarizer. Especially, do not use the following:

- Water
- Ketone
- Aromatic solvents

10.1.6 Do not attempt to disassemble the LCD Module.

10.1.7 If the logic circuit power is off, do not apply the input signals.

10.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

10.1.8.1 Be sure to ground the body when handling the LCD Modules.
Tools required for assembly, such as soldering irons, must be properly ground.

10.1.8.2 To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

10.1.8.3 The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

### 10.2 Storage Precautions

10.2.1When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

10.2.2The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is: Temperature : 0℃ ～ 40℃ Relatively humidity: ≤80%

10.2.3The LCD modules should be stored in the room without acid, alkali and harmful gas.

### 10.3Transportation Precautions

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.