

深圳市高信技术有限公司

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|---------------|
| PRODUCT GROUP |
| TFT-LCD       |

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| REV. P0 |
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MODULE NO: GX1011S20217-TDDI

CUSTOMER : \_\_\_\_\_

APPROVED BY CUSTOMER

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| Approved by |
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| Remark |
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APPROVED BY GX

Prepared by

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| Checked by |
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[illegible]

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(√) Final specification

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## 1. GENERAL DESCRIPTION

### 1.1 Introduction

GX1011S20217-TDDI is a color active matrix TFT LCD Model using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This Model has a 10.21 inch diagonally measured active area with 440\*1920 resolutions (440 horizontal by 1920 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 16.7M colors.

440\*1920

Sources IC

MIPI Connector

### 1.2 Features

- 8-bit color depth, display 16. 7M colors
- Thin and light weight
- High luminance and contrast ratio, low reflection and wide viewing angle
- RoHS Compliant
- Landscape and Portrait usage support

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## 1.3 Application

- Portable DVD
- Digital picture frame
- Smart home appliances

## 1.4 General Specification

< Table 1. General Specifications >

| Parameter                  | Specification               | Unit              | Remarks |
|----------------------------|-----------------------------|-------------------|---------|
| Outline Dimension          | 64.78(H)*266.04 (V)*4.55(B) | mm                |         |
| Active Area                | 57.95(H) ×252.86(V)         | mm                |         |
| Number Of Pixels           | 440(H) RGB x 1920(V)        | pixels            |         |
| Pixel Pitch                | 43.9(H)×3×131.7(V)          | μm                |         |
| Pixel Arrangement          | RGB Vertical Stripe         |                   |         |
| Display Mode               | Normally Black              |                   |         |
| Display Colors             | 16.7 M                      | colors            |         |
| Average Luminous Intensity | 700                         | cd/m <sup>2</sup> |         |
| Viewing Angle(CR>10)       | 85/85/85/85 (Typ.)          | deg.              |         |
| Color Gamut                | 70                          | %                 |         |
| POL                        | AG5                         |                   |         |
| Interface                  | 4-lane MIPI                 |                   |         |

## 2. ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

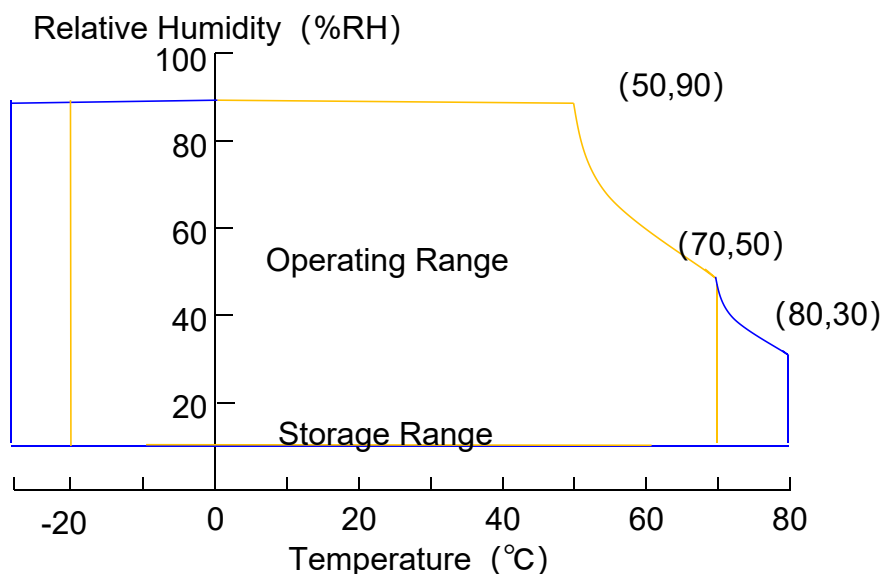
< Table 2. Environment Absolute Maximum Ratings> [Ta =25±2 °C]

| Parameter                  | Symbol          | Min. | Max. | Unit | Remark     |
|----------------------------|-----------------|------|------|------|------------|
| Power Supply Voltage       | VDD             | 3    | 3.6  | V    | Ta = 25 °C |
| Operating Temperature      | T <sub>OP</sub> | -20  | +70  | °C   | Note 1     |
| Storage Temperature        | T <sub>ST</sub> | -30  | +80  | °C   |            |
| Operating Ambient Humidity | H <sub>OP</sub> | 10   | 90   | %RH  |            |
| Storage Humidity           | H <sub>ST</sub> | 10   | 90   | %RH  |            |

Note : 1) Temperature and relative humidity range are shown in the figure below.

Wet bulb temperature should be 39 °C max. and no condensation of water.

T<sub>SUR</sub> : Panel surface Temperature is measured at 50°C Dry Condition



## 3. ELECTRICAL SPECIFICATIONS

### 3.1 TFT LCD Module

< Table 3. Open Cell Electrical Specifications >

[Ta =25±2 °C]

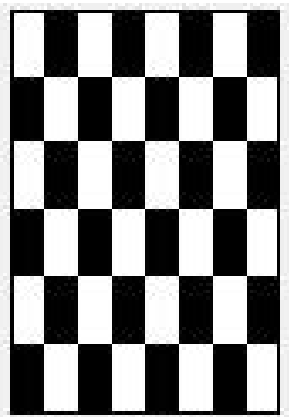
| Parameter                   | Symbol | Values |       |      | Unit | Notes  |
|-----------------------------|--------|--------|-------|------|------|--------|
|                             |        | Min.   | Typ.  | Max. |      |        |
| Power Supply Voltage        | VDD    | 3.0    | 3.3   | 3.6  | V    | Note 1 |
| Power Supply Ripple Voltage | VRP    | -      | -     | 100  | mV   |        |
| Power Supply Current        | IDD    | -      | 40    | -    | mA   |        |
| Analog Operating voltage    | VSP    | 4.5    | 5     | 5    | V    |        |
| Analog Operating voltage    | VSN    | -6.0   | -5    | -4.5 | V    |        |
| Analog Operating voltage    | VCOM   | -1.5   | -0.78 | 0    | V    |        |

Notes : 1. The supply voltage is measured and specified at the interface connector of LCM.

The current draw and power consumption specified is for VBAT=3.2V, Frame rate  $f_v=60\text{Hz}$  and Clock frequency = 71MHz. Test Pattern of power supply current

a) Typ : Mosaic 10 x 5 Pattern(L0/L255)

b) Max : White



|              |                          |         |                 |
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3.2 LED driver

< Table 3.2 LED Driving guideline specifications > Ta=25+/-2°C

| Parameter          | Symbol | Values |      |      | Unit  | Notes |
|--------------------|--------|--------|------|------|-------|-------|
|                    |        | Min.   | Typ. | Max. |       |       |
| BLU Supply Voltage | Vled   | 22     | 24   | 28   | V     |       |
| BLU Supply Current | Iled   |        | 120  |      | mA    |       |
| Number of LED      | -      | 24     |      |      | Piece |       |

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## 4. INTERFACE CONNECTION

< Table4. Pin Assignment for Connector > ( Recommended Connector type: AFC01-S40FCA-00)

| Pin No | Symbol | Description                            | Pin No | Symbol | Description                                   |
|--------|--------|----------------------------------------|--------|--------|-----------------------------------------------|
| 1      | GND    | Ground                                 | 21     | NC     | No Connect                                    |
| 2      | D0P    | MIPI Positive Transmission data input  | 22     | NC     | No Connect                                    |
| 3      | D0N    | MIPI Negative Transmission data input  | 23     | NC     | No Connect                                    |
| 4      | GND    | Ground                                 | 24     | RESET  | RESET pin +3.3V                               |
| 5      | D1P    | MIPI Positive Transmission data input  | 25     | NC     | No Connect                                    |
| 6      | D1N    | MIPI Negative Transmission data input  | 26     | NC     | No Connect                                    |
| 7      | GND    | Ground                                 | 27     | GND    | Ground                                        |
| 8      | CLKP   | MIPI Positive Transmission clock input | 28     | LEDK   | LED Negative                                  |
| 9      | CLKN   | MIPI Negative Transmission clock input | 29     | LEDK   | LED Negative                                  |
| 10     | GND    | Ground                                 | 30     | GND    | Ground                                        |
| 11     | D2P    | MIPI Positive Transmission data input  | 31     | NC     | No Connect                                    |
| 12     | D2N    | MIPI Negative Transmission data input  | 32     | GND    | Ground                                        |
| 13     | GND    | Ground                                 | 33     | GND    | Ground                                        |
| 14     | D3P    | MIPI Positive Transmission data input  | 34     | NC     | No Connect                                    |
| 15     | D3N    | MIPI Negative Transmission data input  | 35     | LEDA   | LED Positive                                  |
| 16     | GND    | Ground                                 | 36     | LEDA   | LED Positive                                  |
| 17     | GND    | Ground                                 | 37     | GND    | Ground                                        |
| 18     | NC     | No Connect                             | 38     | VCC    | Power supply for digital circuits +3.3V input |
| 19     | NC     | No Connect                             | 39     | VCC    | Power supply for digital circuits +3.3V input |
| 20     | NC     | No Connect                             | 40     | NC     | No Connect                                    |

Table Pin Assignments for theTP( Recommended Connector type: AFC01-S06FCA-00)

| PIN | SYMBOL  | I/O | Description                     | Remark |
|-----|---------|-----|---------------------------------|--------|
| 1   | TP_SCL  | I   | I2C interface clock pin (+3.3V) |        |
| 2   | TP_SDA  | I   | I2C interface data pin (+3.3V)  |        |
| 3   | NC      | -   | No connection.                  |        |
| 4   | TP_RESX | I   | External reset for TP (+3.3V)   |        |
| 5   | TP_INT  | I   | Touch screen interrupt (+3.3V)  |        |
| 6   | GND     | P   | Ground                          |        |

## 5. Interface timing Parameter

### MIPI DC Characteristic

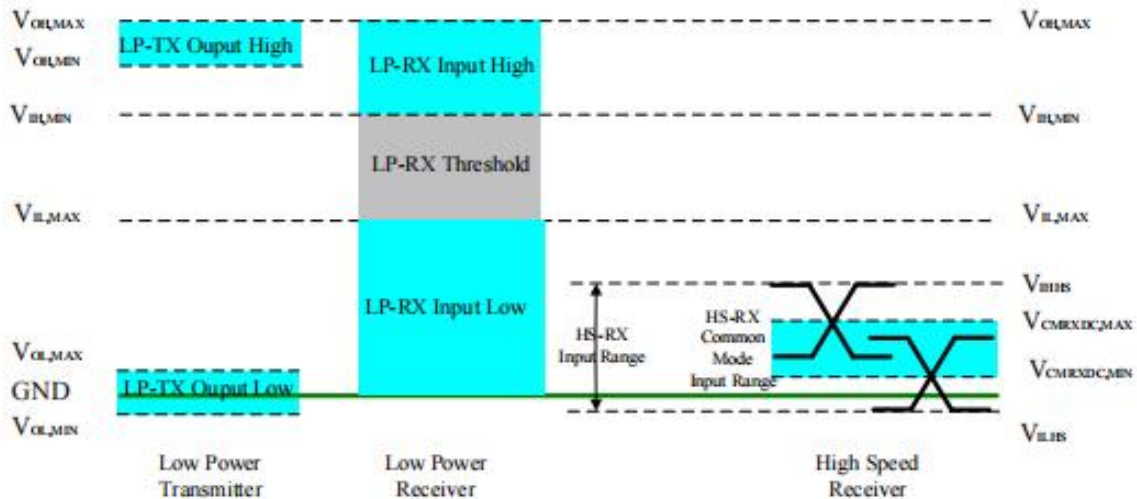


Figure 76 MIPI Signaling Voltage Levels

| Parameter                                    | Symbol  | Specification |     |      | Unit |
|----------------------------------------------|---------|---------------|-----|------|------|
|                                              |         | MIN           | TYP | MAX  |      |
| Operation Voltage for MIPI Receiver          |         |               |     |      |      |
| Low power mode operating voltage             | VLPH    | -             | 1.2 | -    | V    |
| MIPI Characteristics for High Speed Receiver |         |               |     |      |      |
| Single-ended input low voltage               | VILHS   | -40           | -   | -    | mV   |
| Single-ended input high voltage              | VIHHS   | -             | -   | 460  | mV   |
| Common-mode voltage                          | VCMRXDC | 70            | -   | 330  | mV   |
| Differential input impedance                 | ZID     | 80            | 100 | 125  | ohm  |
| MIPI Characteristics for Low Power Mode      |         |               |     |      |      |
| Pad signal voltage range                     | VI      | -50           | -   | 1350 | mV   |
| Logic 0 input threshold                      | VIL     | 0             | -   | 550  | mV   |
| Logic 1 input threshold                      | VIH     | 880           | -   | -    | mV   |
| Output low level                             | VOL     | -50           | -   | 50   | mV   |
| Output high level                            | VOH     | 1.1           | 1.2 | 1.3  | V    |

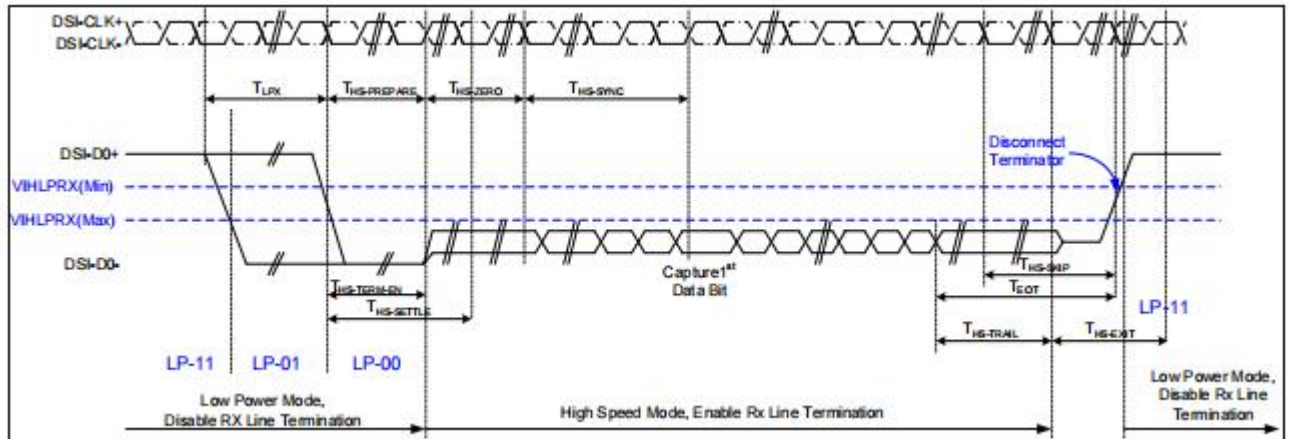
## AC Characteristics

### MIPI Timing



Figure 77 High Speed Mode – Clock Channel Timing

| Signal      | Symbol                 | Parameter                | Specification |     |     | Unit | Description |
|-------------|------------------------|--------------------------|---------------|-----|-----|------|-------------|
|             |                        |                          | MIN           | TYP | MAX |      |             |
| DSI-CLK+/-  | $2xU_{INST}$           | Double UI instantaneous  | 1.6           | -   | 10  | ns   |             |
| DSI-CLK+/-  | $U_{INSTA}, U_{INSTB}$ | UI instantaneous half    | 0.8           | -   | 5   | ns   |             |
| fDSI-CLK+/- | $F_{DSICLK}$           | DSI-CLK+/- frequency     | 100           | -   | 625 | MHz  |             |
| DSI-Dn+/-   | $T_{DS}$               | Data to clock setup time | 0.15          | -   | -   | UI   |             |
| DSI-Dn+/-   | $T_{DH}$               | Data to clock hold time  | 0.15          | -   | -   | UI   |             |



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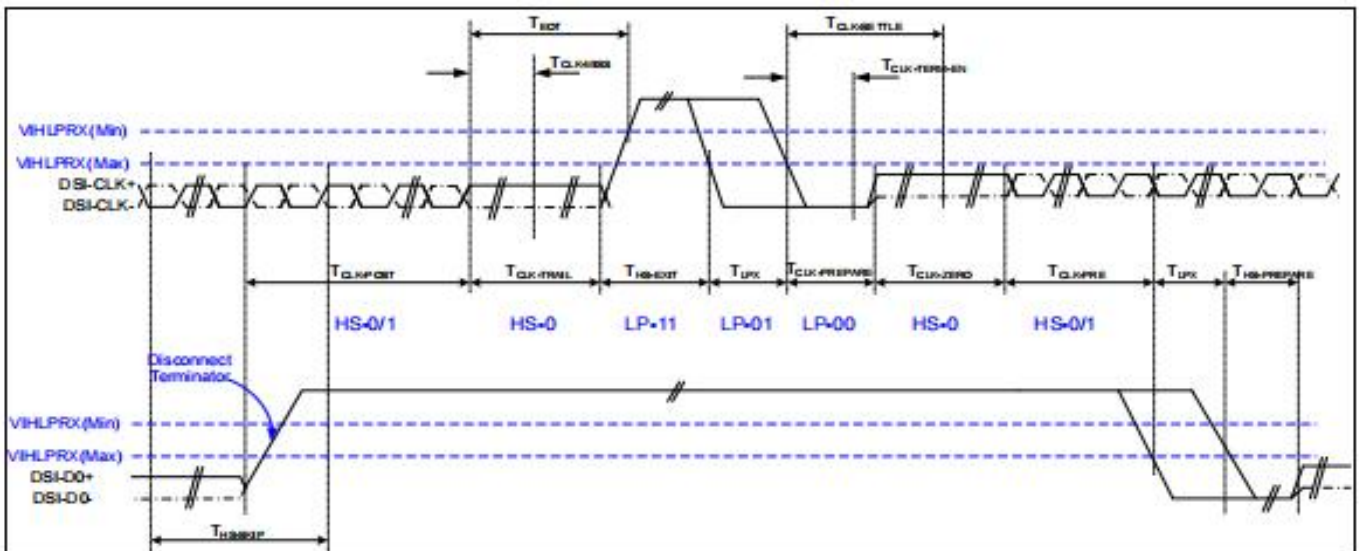
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| Parameter                                                                                                                                                                                                                                                                                                           | Symbol           | Specification |     |          | Unit |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|---------------|-----|----------|------|
|                                                                                                                                                                                                                                                                                                                     |                  | MIN           | TYP | MAX      |      |
| Time to drive LP-00 to prepare for HS transmission                                                                                                                                                                                                                                                                  | $T_{HS-PREPARE}$ | 40+4UI        | -   | 85+6UI   | ns   |
| Time from start of t HS-TRAIL or t CLK-TRAIL period to start of LP-11 state                                                                                                                                                                                                                                         | $T_{EOT}$        | -             | -   | 105+12UI | ns   |
| Time to enable data receiver line termination measured from when Dn crosses VILMAX                                                                                                                                                                                                                                  | $T_{HS-TERM-EN}$ | -             | -   | 35+4UI   | ns   |
| Time to drive flipped differential state after last payload data bit of a HS transmission                                                                                                                                                                                                                           | $T_{HS-TRAIL}$   | 60+4UI        | -   | -        | ns   |
| Time-out at RX to ignore transition period of EoT                                                                                                                                                                                                                                                                   | $T_{HS-SKIP}$    | 40            | -   | 145+10UI | ns   |
| Time to drive LP-11 after HS burst                                                                                                                                                                                                                                                                                  | $T_{HS-EXIT}$    | 100           | -   | -        | ns   |
| Length of any Low-Power state period                                                                                                                                                                                                                                                                                | $T_{LPX}$        | 50            | -   | -        | ns   |
| Sync sequence period                                                                                                                                                                                                                                                                                                | $T_{HS-SYNC}$    | -             | 8UI | -        | ns   |
| Minimum lead HS-0 drive period before the Sync sequence                                                                                                                                                                                                                                                             | $T_{HS-ZERO}$    | 105+6UI       | -   | -        | ns   |
| Time interval during which the HS receiver should ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PREPARE}$                                                                                                                                                                            | $T_{CLK-SETTLE}$ | 95            | -   | 300      | ns   |
| Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HS-PREPARE}$ .<br>The HS receiver shall ignore any Data Lane transitions before the minimum value, and the HS receiver shall respond to any Data Lane transitions after the maximum value. | $T_{HS-SETTLE}$  | 85+6UI        | -   | 145+10UI | ns   |



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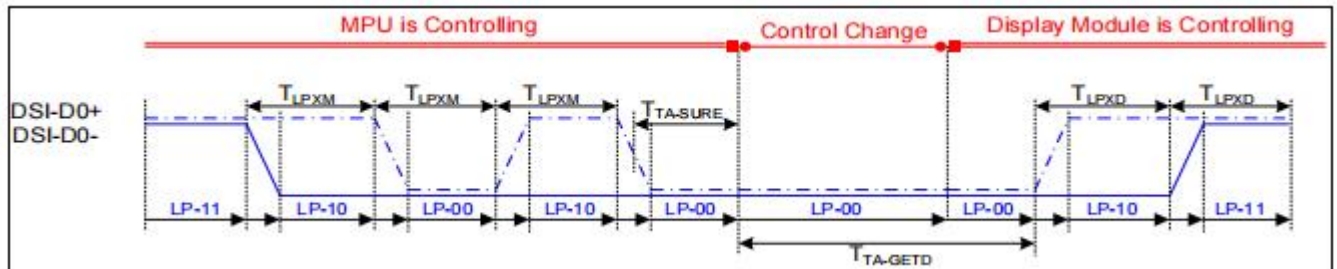
| Parameter                                                                                                                  | Symbol                           | Specification |     |     | Unit |
|----------------------------------------------------------------------------------------------------------------------------|----------------------------------|---------------|-----|-----|------|
|                                                                                                                            |                                  | MIN           | TYP | MAX |      |
| Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode  | $T_{CLK-POST}$                   | 60+52UI       | -   | -   | ns   |
| Detection time that the clock has stopped toggling                                                                         | $T_{CLK-MISS}$                   | -             | -   | 60  | ns   |
| Time to drive LP-00 to prepare for HS clock transmission                                                                   | $T_{CLK-PREPARE}$                | 38            | -   | 95  | ns   |
| Minimum lead HS-0 drive period before starting Clock                                                                       | $T_{CLK-PREPARE} + T_{CLK-ZERO}$ | 300           | -   | -   | ns   |
| Time to enable Clock Lane receiver line termination measured from when Dn cross VIL,MAX                                    | $T_{CLK-TERM-EN}$                | -             | -   | 38  | ns   |
| Minimum time that the HS clock must be set prior to any associated data lane beginning the transmission from LP to HS mode | $T_{CLK-PRE}$                    | 8             | -   | -   | UI   |
| Time to drive HS differential state after last payload clock bit of a HS transmission burst                                | $T_{CLK-TRAIL}$                  | 60            | -   | -   | ns   |

Note: 3-Lane =  $(1000 / f_{mipi} * 8 * 52 - T_{HS\_TRAIL} - 60) / (1000 / f_{mipi})$

4-Lane =  $(1000 / f_{mipi} * 8 * 39 - T_{HS\_TRAIL} - 60) / (1000 / f_{mipi})$

Example: 3-Lane, 600Mbps :  $n = (1000 / 600 * 8 * 52 - T_{HS\_TRAIL} - 60) / (1000 / 600) = 340$

4-Lane, 600Mbps :  $n = (1000 / 600 * 8 * 39 - T_{HS\_TRAIL} - 60) / (1000 / 600) = 236$



| Parameter                                                                   | Symbol          | Specification |             |             | Unit |
|-----------------------------------------------------------------------------|-----------------|---------------|-------------|-------------|------|
|                                                                             |                 | MIN           | TYP         | MAX         |      |
| Length of any Low-Power state period : Master side                          | $T_{LPX}$       | 50            | -           | 75          | ns   |
| Length of any Low-Power state period : Slave side                           | $T_{LPX}$       | 47.5          | -           | 52.5        | ns   |
| Ratio of $T_{LPX}$ (MASTER) $T_{LPX}$ (SLAVE) between Master and Slave side | Ratio $T_{LPX}$ | 2/3           | -           | 2/3         |      |
| Time-out before new TX side start driving                                   | $T_{TA-SURE}$   | $T_{LPX}$     | -           | $2 T_{LPX}$ | ns   |
| Time to drive LP-00 by new TX                                               | $T_{TA-GETD}$   | -             | $5 T_{LPX}$ | -           | ns   |
| Time to drive LP-00 after Turnaround Request                                | $T_{TA-GETD}$   | -             | $4 T_{LPX}$ | -           | ns   |

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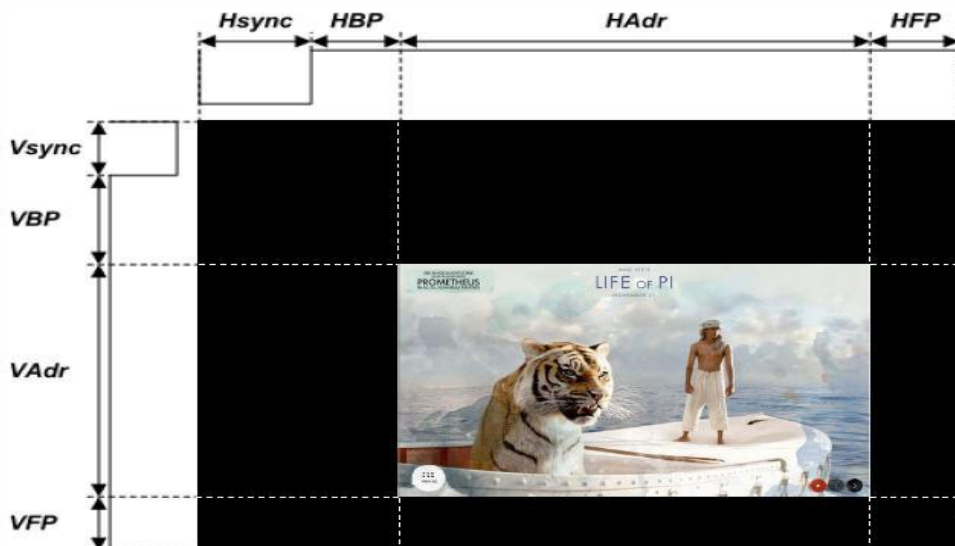
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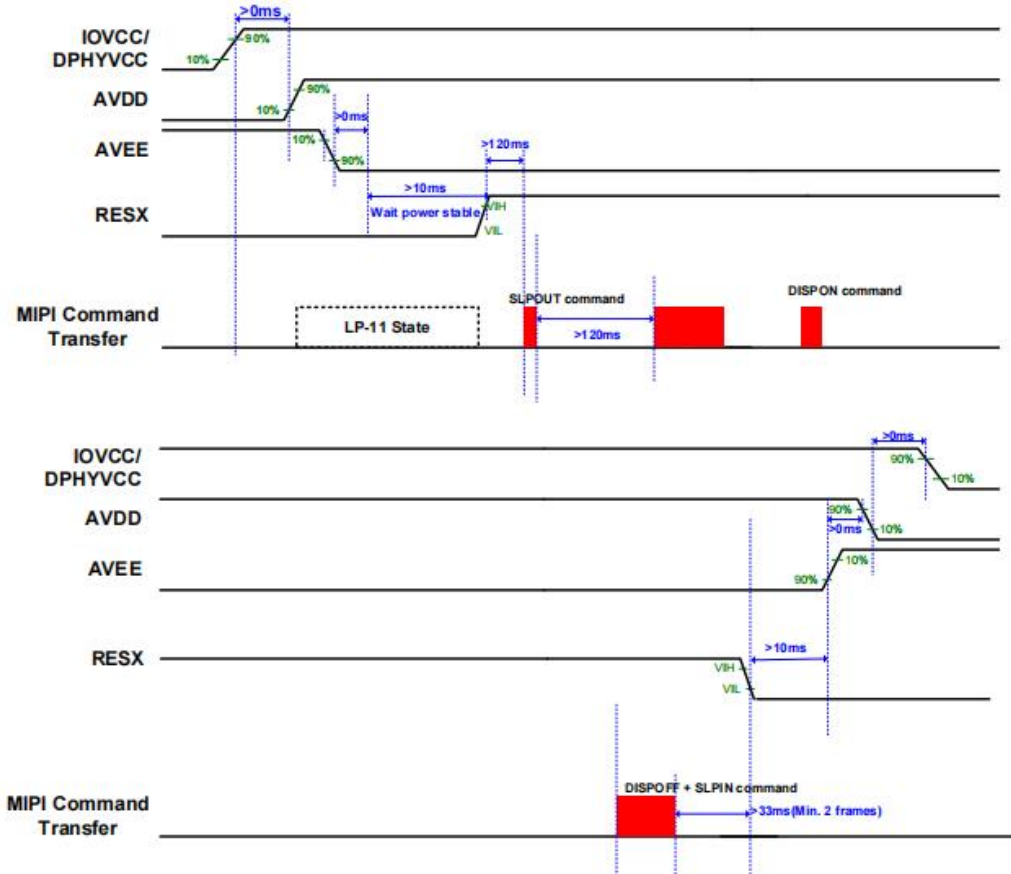
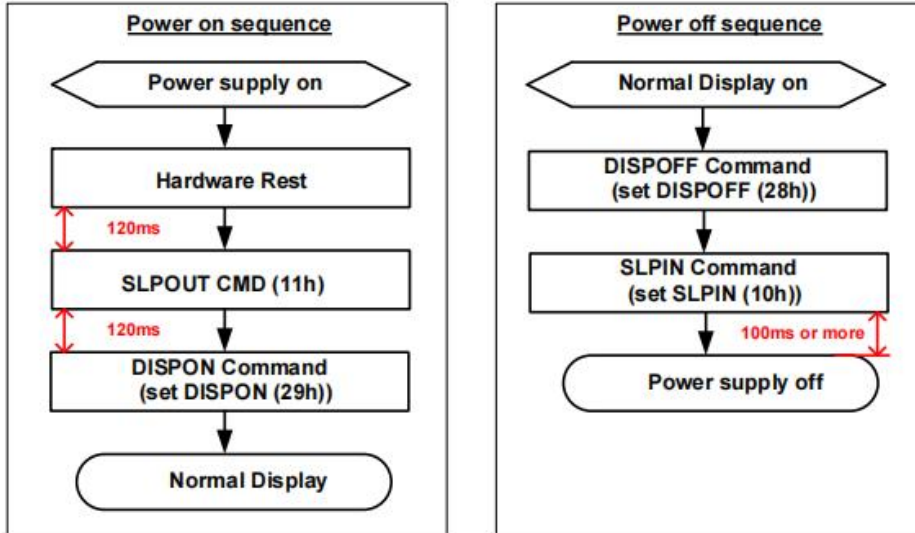
< Table 5. Timing Parameter >

| Item   |            |                        | Symbol | min  | typ  | max  | UNIT             |
|--------|------------|------------------------|--------|------|------|------|------------------|
| LCD    | Frame Rate |                        | -      | -    | 60   | -    | Hz               |
| Timing | DCLK       | Frequency              | fCLK   | -    | 71   | -    | MHz              |
|        | Horizontal | Horizontal total time  | tHP    | -    | 540  | -    | t <sub>CLK</sub> |
|        |            | Horizontal Active time | tHadr  | 440  |      |      | t <sub>CLK</sub> |
|        |            | Horizontal Pulse Width | tHsync | -    | 20   | -    | t <sub>CLK</sub> |
|        |            | Horizontal Back Porch  | tHBP   | -    | 40   | -    | t <sub>CLK</sub> |
|        |            | Horizontal Front Porch | tHFP   | -    | 40   | -    | t <sub>CLK</sub> |
|        | Vertical   | Vertical total time    | tvp    | -    | 2009 | -    | t <sub>H</sub>   |
|        |            | Vertical Active time   | tVadr  | 1920 |      |      | t <sub>H</sub>   |
|        |            | Vertical Pulse Width   | tVsync | -    | 4    | -    | t <sub>H</sub>   |
|        |            | Vertical Back Porch    | tVBP   | -    | 12   | -    | t <sub>H</sub>   |
|        |            | Vertical Front Porch   | tVFP   | -    | 273  | -    | t <sub>H</sub>   |
| Lane   |            |                        | -      | 4    | -    | Lane |                  |



## 6. POWER SEQUENCE

The power On/Off sequence is illustrated below.



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## 7. OPTICAL SPECIFICATION

### 7.1 Overview

The test of view angle range shall be measured in a dark room (ambient luminance  $\leq 1\text{lux}$  and temperature =  $25\pm 2^\circ\text{C}$ ) with the equipment of Luminance meter system (Goniometer system and TOPCON CS2000/CA310) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of  $\theta$  and  $\Phi$  equal to  $0^\circ$ . We refer to  $\theta\Phi=0$  ( $=\theta_3$ ) as the 3 o'clock direction (the "right"),  $\theta\Phi=90$  ( $=\theta_{12}$ ) as the 12 o'clock direction ("upward"),  $\theta\Phi=180$  ( $=\theta_9$ ) as the 9 o'clock direction ("left") and  $\theta\Phi=270$  ( $=\theta_6$ ) as the 6 o'clock direction ("bottom"). While scanning  $\theta$  and/or  $\Phi$ , the center of the measuring spot on the Display surface shall stay fixed. The luminance, color and uniformity (etc) should be tested by CS2000/CA310. The backlight should be operating for 10 minutes prior to measurement. VDD shall be  $3.3 \pm 0.3\text{V}$  at  $25^\circ\text{C}$ . Optimum viewing angle direction is 6 'clock

<Table 7. Optical Specifications>

| Parameter                  |            | Symbol        | Condition                      | Min.  | Typ.  | Max.  | Unit              | Remark |
|----------------------------|------------|---------------|--------------------------------|-------|-------|-------|-------------------|--------|
| Viewing Angle Range        | Horizontal | $\Theta_3$    | CR > 10                        | 80    | 85    | -     | Deg.              |        |
|                            |            | $\Theta_9$    |                                | 80    | 85    | -     | Deg.              |        |
|                            | Vertical   | $\Theta_{12}$ |                                | 80    | 85    | -     | Deg.              |        |
|                            |            | $\Theta_6$    |                                | 80    | 85    | -     | Deg.              |        |
| Contrast Ratio             |            | CR            | $\Theta = 0^\circ$             | 800   | 1000  | -     |                   |        |
| Average Luminous Intensity |            |               |                                | 600   | 700   |       | cd/m <sup>2</sup> |        |
| Reproduction of color      |            | Rx            | $\Theta = 0^\circ$             | 0.629 | 0.659 | 0.689 |                   |        |
|                            |            | Ry            |                                | 0.288 | 0.318 | 0.348 |                   |        |
|                            |            | Gx            |                                | 0.233 | 0.263 | 0.293 |                   |        |
|                            |            | Gy            |                                | 0.538 | 0.568 | 0.598 |                   |        |
|                            |            | Bx            |                                | 0.107 | 0.137 | 0.167 |                   |        |
|                            |            | By            |                                | 0.054 | 0.084 | 0.114 |                   |        |
|                            |            | Wx            |                                | 0.275 | 0.305 | 0.335 |                   |        |
|                            |            | Wy            |                                | 0.303 | 0.333 | 0.363 |                   |        |
| Color Gamut                |            |               | $\Theta = 0^\circ$             | 65    | 70    | -     | %                 |        |
| Response Time              |            | Tr            | Ta= 25°C<br>$\Theta = 0^\circ$ | -     | 30    | 35    | ms                |        |
|                            |            | Tf            |                                | -     |       |       | ms                |        |
|                            |            | Tgray         |                                | -     | -     | -     | ms                |        |

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Notes : 1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see FIGURE 1).

2. Contrast measurements shall be made at viewing angle of  $\Theta = 0$  and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see FIGURE 2) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. The color chromaticity coordinates specified in Table 5. shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.
4. The electro-optical response time measurements shall be made as FIGURE 2 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is  $T_r$ , and 90% to 10% is  $T_d$ .

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7.2 Optical measurements

Figure 1:The definition of Viewing Angle

Refer to the graph below marked by  $\theta$  and  $\phi$ .

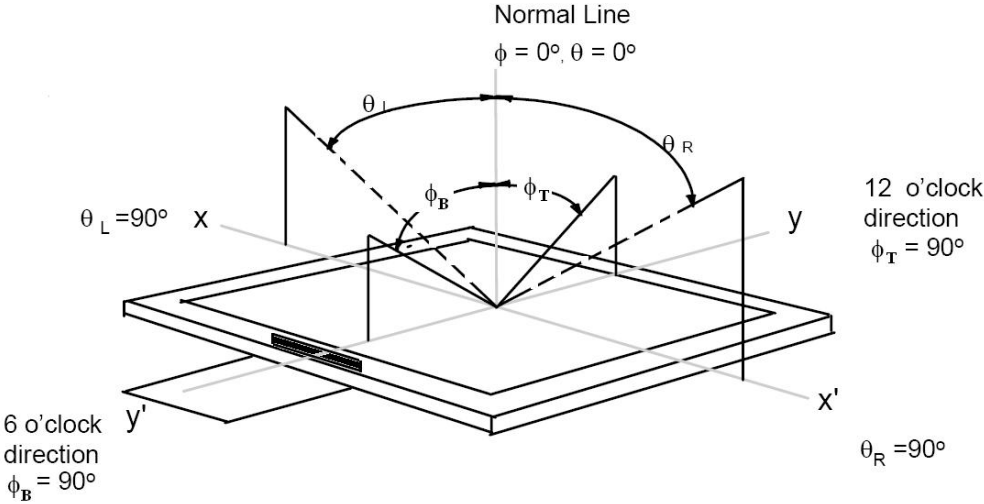
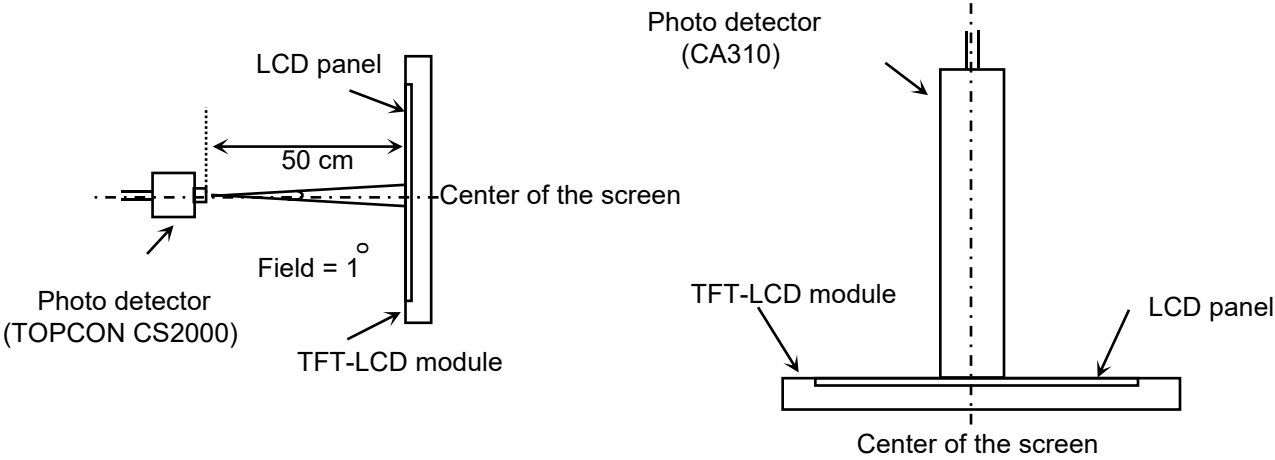


Figure 2. Measurement Set Up



View angel range, uniformity, etc. measurement setup      Flicker, measurement setup

[illegible]

Figure 4:

Viewing direction is normal user viewing direction which is vertical to the display surface

- The polarizer which is closer to viewer is defined as Front Polarizer
- The polarizer which is on the rear side of viewer is defined as Rear Polarizer
- The X axis is defined as parallel line to top & bottom sidelines of the Active Area
- PdF which is marked in blue arrow is polarization degree of Front polarizer
- PdR which is marked in red arrow is polarization degree of Back polarizer
- The polarization degree parameter must be indicated in range of 0deg to 180deg according to above definition

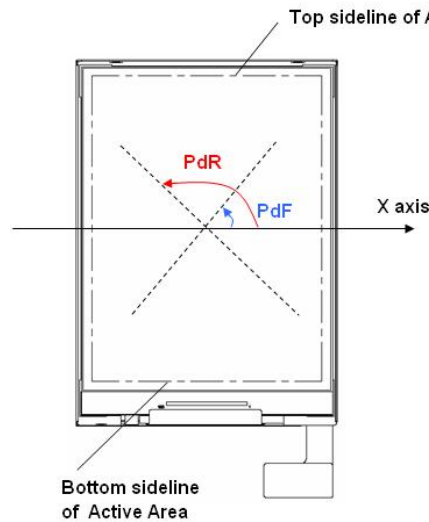
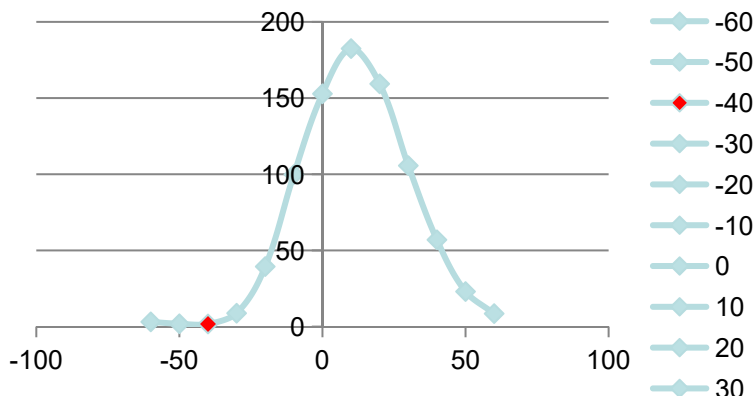


Figure.5:

Using luminance test method.

- Test pattern : 128 gray
- If the viewing direction is 12 o'clock ,then test the luminance while  $\theta = -60^\circ, \theta = -50^\circ, \theta = -40^\circ, \theta = -30^\circ, \theta = -20^\circ, \theta = -10^\circ, \theta = 0^\circ, \theta = 10^\circ, \theta = 20^\circ, \theta = 30^\circ, \theta = 40^\circ, \theta = 50^\circ, \theta = 60^\circ$ . The luminance test as figure below:



8. Mechanical Characteristics

As shown in Table 8.

< Table 8 Dimensional Parameters >

| Parameter           | Specification                                  | Unit   |
|---------------------|------------------------------------------------|--------|
| Dimensional outline | 64.78(H)*266.04 (V)*4.55(B)                    | mm     |
| Active area         | 57.95(H) ×252.86(V)                            | mm     |
| Pixel pitch         | 43.9(H)×3×131.7(V)                             | μm     |
| Number of pixels    | 440(H) RGB x 1920(V) 1 pixel = R + G + B dots) | pixels |

## 9. RELIABILITY TEST

The Reliability test items and its conditions are shown in below.

<Table 9. Reliability test>

| No | Test Items                                      | Conditions                            |
|----|-------------------------------------------------|---------------------------------------|
| 1  | High temperature storage test                   | Ta = 80°C, 240 hrs                    |
| 2  | Low temperature storage test                    | Ta = -30 °C, 240 hrs                  |
| 3  | High temperature operation test                 | Ta = 70°C, 240 hrs                    |
| 4  | Low temperature operation test                  | Ta = -20 °C, 240 hrs                  |
| 5  | High temperature & high humidity operation test | Ta = 60 °C, 90%RH,240hrs              |
| 6  | Thermal shock                                   | Ta = -30 °C ↔ 80°C (0.5 hr), 50 cycle |

Note : After the reliability test, the product only guarantee function normally without any fatal defect (non-display, line defect, abnormal display etc ). All the cosmetic specification is judged before the reliability test.

|              |                          |         |                  |
|--------------|--------------------------|---------|------------------|
|              |                          |         |                  |
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## 10. Handling & Cautions

Please pay attention to the followings when you use this TFT LCD open cell (OC) .

### 10.1 Mounting Precautions

- Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
- You must mount an OC using specified mounting holes (Details refer to the drawings).
- You should consider the mounting structure so that uneven force (ex. Twisted stress, Concentrated stress) is not applied to the OC. And the case on which an OC is mounted should have sufficient strength so that external force is not transmitted directly to the OC.
- Do not apply mechanical stress or static pressure on OC; Abnormal display cause by pressing some parts of OC during assembly process , do not belong to product failure, the press should be agreed by two sides.
- Determine the optimum mounting angle, refer to the viewing angle range in the specification for each model.
- Do not apply mechanical stress or static pressure on OC , and avoid impact, vibration and falling.
- Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
- Protection film for polarizer on the OC should be slowly peeled off before display.
- Be careful to prevent water & chemicals contact the OC surface.
- You should adopt radiation structure to satisfy the temperature specification.
- Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are detrimental to the polarizer.)

- When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzine. Normal-hexane & alcohol is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene , because they cause chemical damage to the polarizer.
- Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
- This OC has its circuitry PCBs on the front or rear side and Driver IC, should be handled carefully in order not to be stressed.
- Avoid impose stress on PCB and Driver IC during assembly process ,Do not drawing, bending, COF package & wire.
- Do not disassemble the OC.

## 10.2 Operating Precautions

- Do not connect or disconnect the cable to/from the OC at the “Power On” Condition.
- When the OC is operating, do not lose CLK, ENAB signals. If any one of these signals is lost, the OC would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the OC would be damaged.
- Do not allow to adjust the adjustable resistance or switch.
- The electrochemical reaction caused by DC voltage will lead to LCD open cell degradation, so DC drive should be avoided.
- The LCD panel use C-MOS LSI drivers, so customers are recommended that any unused input terminal would be connected to Vdd or Vss, do not input any signals before power is turn on, and ground you body, work/assembly area, assembly equipment to protect against static electricity.
- Do not exceed the absolute maximum rating value. (supply voltage variation, input voltage variation, variation in part contents and environmental temperature, and so on) Otherwise the OC may be damaged.
- OC has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.

11.Appendix Outline

